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TESSERA 3.3-018Serial No.  
08/030,194

## LIST OF PRIOR ART CITED BY APPLICANT

(Use several sheets if necessary)

Applicant  
KHANDROS ET AL

Filing Date: APRIL 28, 1993

Group 2503

## U.S. PATENT DOCUMENTS

*EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
SVC	AA	4,658,332	4/87	BAKER ET AL			
SVC	AB	4,847,146	7/89	YEH ET AL			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

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## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	AL							
	AM							
	AN							
	AO							
	AP							

## OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

SVC	✓	AR	"Design For Minimum Chip Joint Stress", IBM TECHNICAL DISCLOSURE BULLETIN, Vol. 32, No. 7, December 1989
SVC	✓	AS	"Improved C4 Reliability Using Low Modulus Dielectric Layer", IBM TECHNICAL DISCLOSURE BULLETIN, Vol. 32, No. 6A, November 1989
		AT	
EXAMINER		DATE CONSIDERED	
S. C. Clark		7-7-96	

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.